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The sense of the workshop attendees was that CMOS will continue to serve as the mainstream technology for information processing for the foreseeable future. The exponential progress in semiconductor technology characterized by Moore's Law will also continue until at least 0.1 microns, after which there is the possibility that the rate of progress will slow due to the numerous technical challenges that must be overcome. According to Dr. Bob Doering of Texas Instruments, the International Technology Roadmap for Semiconductors, to be published in 1999 (ITRS '99), identifies many of the difficult technical challenges that must be overcome to sustain the historical rate of progress for CMOS technology

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The Third International Workshop on Future Information Processing Technologies
Harrison Hot Springs, B.C., Canada; August 24-27, 1999

I. Project Activities and Findings

The sense of the workshop attendees was that CMOS will continue to serve as the mainstream technology for information processing for the foreseeable future. The exponential progress in semiconductor technology characterized by Moore's Law will also continue until at least 0.1 microns, after which there is the possibility that the rate of progress will slow due to the numerous technical challenges that must be overcome. According to Dr. Bob Doering of Texas Instruments, the International Technology Roadmap for Semiconductors, to be published in 1999 (ITRS '99), identifies many of the difficult technical challenges that must be overcome to sustain the historical rate of progress for CMOS technology. For example:

i) the performance of MOS transistors is gradually degrading with dimensional scaling due to increases in off-current and decreasing drive current capability,
ii) long on-chip interconnects offer delays comparable to or exceeding device switching times,
iii) patterning issues will require substantial investment of resources and effort to support sub 100 nanometer features,
iv) the higher rate of growth of fabrication facility costs relative to market demand growth is forcing structural changes by the industry,
v) portable applications have led to requirements to reduce chip power consumption and to develop new, cost-effective, system level integration technologies
vi) design productivity has not kept pace with growth in technology capabilities, and
vii) test of extraordinarily complex chips with diverse classes of signals is increasingly difficult.

In spite of the many challenges to sustaining the exponential progress of CMOS technology, there was general optimism at the workshop that many of the barriers that we can now foresee will be overcome or circumvented by the industry. Dr. Armin Wieder of Infineon Technologies offered a possible vision for technology change in response to the above technical challenges. His vision of possible responses are summarized by Table 1 below:

Technology	Now	Future	Discontinuity timing
Material	Silicon	Silicon + Add-Ins and Add-Ons	
Processing	Planar Technology	3D Technology	Major discontinuity 2015
Devices	Statistical electron control	Individual electron control	Major discontinuity 2015
Circuits	Noise suppression	Noise tolerance	
Systems	Programmed system	Learning system	Major discontinuity 2015
Packaging	Die level packaging	Wafer level array assembly	
CAX	Tools (Fast simulation)	Schools (Fast training)	
Test	External test	Build-in self test and repair	Major discontinuity 2015
Manufacturing	Clean room	Vacuum manufacturing	Major discontinuity 2015
Applications	Development oriented	Application science (Machine adapts to humans)	

Table 1. Projections for Change in Semiconductor Technologies

It turns out that there are also equivalent 'Moore's Laws' in other sustaining information processing technologies, e.g., photonics for optical transmission systems, magnetic storage devices, etc. For example, the demand in Japan for data transmission services is growing at an exponential rate, according to Dr. Yukou Mochida of Fijitsu Laboratories, and this demand is

being met by equivalent growth in the capability of photonic networks. This general phenomenon led Dr. Martin Schumann of Philips to offer a generalized Moore's Law for Technology:

All characteristic parameters of information processing technologies improve by a factor of two every one and one-half to three years.

Dr. Schuurmann suggested that the notion of 'Ambient Intelligence' an integrated technology whose components are ubiquitous communication, distributed computing, and intelligent user interaction, is a likely consequence of the extraordinary growth in information processing technology capability. This is a very general concept in which machines are embodied with forms of intelligence and have the capability to communicate with other machines in the performance of their services for users.

Dr. Paul Jay of Nortel Networks pointed out that an incumbent technology is vulnerable when there is a performance overshoot compared to what markets demand or absorb[1]. In this spirit, it could be that the growth in non-digital function on chip could lead to an emphasis on analog technologies. He suggested that usage of silicon domain may bifurcate with new neural or biologic systems playing an important role in future silicon applications. This projection appears to be supported by the mixed signal character of system-on-a-chip applications.

Dr. Bryan Ackland of Lucent Technologies noted that the the Digital Signal Processing (DSP) market is splitting into two segments; one addressing very high performance applications and the other associated with ultra low power and low cost applications. Next generation infrastructure and embedded applications will require high performance, low cost, low power, and programmability. Many design and technology techniques are being exploited to achieve low power requirements including clock gating, minimization of data transitions, dual V_T transistors, voltage scaling, etc. Performance approaches include Very Long Instruction Word (VLIW) designs, and Multiple Instruction Multiple Data (MIMD) architectures with application specific coprocessors to exploit task level parallelism. The greatest challenge for DSP though is regarded to lie in the area of software tools, e.g., optimizing compilers, debuggers, profilers, Real Time Operating Systems (RTOS) etc.

Dr. K.P. Estola of Nokia described the evolution of wireless terminals, another important and rapidly growing segment of information processing technologies. He indicated that silicon technology is not a limiting problem for Nokia. This market is driven by a very short product life cycle, placing a premium on rapid design cycles and on cost-effective system integration technologies. The methos are not now established for rapid system design including issues such as IP block management, design re-use, and chip interfaces. A particular concern is the design and fabrication of analog parts satisfying specifications such as 120 db dynamic range, 2 volt power supply, and 2 GHz operating frequencies. Rapid progress in the design of CMOS LSI chips to mimic retinal function was reported by Dr. K. Kyuma of Mitsubishi. It now appears that for many applications, CMOS cameras can offer satisfactory performance relative to CCD technology at much lower cost. The theme of the presentation by Dr. M. Fukima from NEC was that programmable LSI chips offer dynamical re-configurabilty to match the specific problem computational requirements and provide a new approach to flexible, high performance computing.

In the session on Atomic/Molecular Information Processing, Dr. S Uemura of ISE Electronics discussed the application of carbon nanotubes as field emitters for large area displays. A screening technique was used to process the randomly oriented array of nanotubes that result from their fabrication, to ensure that emission is sufficiently directed to achieve uniformity and coherence. Dr. Uemura demonstrated working versions of high intensity nanotube field emitters. Dr. A. Ekert of Oxford University gave a status report on quantum computing that reviewed the extraordinary potential advantage of quantum computing relative to conventional Von Neumann

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[1] Clayton M. Christensen, "The Innovators Dilemma"

computing for problems in cryptography that require the factorization of large numbers. While the theory of quantum computing seems to be advancing nicely, our ability to fabricate more than just a few quantum gates is in its infancy. Dr. Ekert described ion traps and NMR techniques that have been used to realize up to seven quantum gates, but substantial technology advances are required to obtain the several thousand quantum gates thought to be required for significant problems. Dr. Phil Keukes of Hewlett Packard described an approach to radically expanding the available number of gates per unit volume by the use of interconnected molecular switches. Functional molecular switches have been designed and implemented. These switches are being extended to handle bipolar switching. The key to the successful application of imperfectly fabricated structures with molecular complexity is to utilize robust interconnect schemes that allow the machine to decide where defective cells are located, and to configure itself to achieve required functionality. Dr. Keukes reported that the Hewlett Packard experience with the TERAMAC computer has provided convincing evidence that this approach is viable.

The session on Non-Traditional Materials/Processes contained a very interesting paper by Dr. K. Yano of Hitachi on single electron memories. By placing islands of silicon in the channel of the MOSFET transistor, a single electron memory device can be created. Dr. Yano reported that, although access times are slower than comparable DRAM devices, competitive levels of memory density can be achieved. One possible application of SEM technology is in the area of embedded memories for integrated on-chip applications. Integrated circuit fabrication is basically a chiseling process where the silicon substrate is modified to achieve the final product. However, one can envision an approach to assembly based on self-organization of molecular building blocks. Dr. David Janes from Purdue University gave an overview of research in self-assembly for nanoelectronics, a new area of endeavor that is beginning to show applicable results. For example, low resistance contacts have been synthesized on LTG GaAs with 10 nm^2 of contact area exhibiting contact resistances of 10^{-6} ohm-cm^2 and greater than 10^6 amp/cm^2 for n type LTG GaAs. Dr. C. Joachim from CEMES continued this theme by discussing some of the essential elements of molecular engineering for nano-electronics. This research is very fundamental and if successful, will offer a myriad of new electronic devices and systems.

The 3rd IWFIPT was dedicated to the memory of Dr. Roger J. Van Overstraeten, a distinguished scientist and leader in information technology research, who was a founding member of the International Organizing Committee for the workshop. The spirit of the 3rd IWFIPT exemplified the vision of Dr. Van Overstraeten and other IWFIPT founders. Approaches to the resolution of technology challenges were discussed openly by participants and there was a sense of commitment to continuing the progress in information processing technologies to which we all have jointly contributed, and to which we owe much.

II. Project Training and Development

The Third International Workshop on Future Information Processing was not designed as a training event. However, as a consequence of the paper and poster discussions that occurred throughout the meeting, attendees were given the opportunity to become familiar with the work of colleagues in related fields throughout the world and to gain insights into future technology directions.

III. Research Training

The primary thrust of the meeting was not to train attendees in research process but rather to identify promising directions for future research. Some of the directions that were identified are:

- Research to extend the life of CMOS technologies to their limit. (Currently projected to be in the 10 nm minimum feature size regime)
  - This work must comprehend the development of new materials and processes to extend bulk planar CMOS, the development of novel MOSFET structures to allow the technology to reach the 10 nm regime, and research to develop fabrication tools, e.g., patterning, for ultimate CMOS.
- Research to develop a broad array of intelligent applications based on semiconductor technology that are ubiquitous and that provide timely services for humankind.

- Research to develop new materials and devices to sustain the Moore's Law progress that has defined the semiconductor industry for the past three decades.
- Is it be possible to effectively continue Moore's Law based on the concept of 'equivalent scaling' wherein system architecture and design innovations are used to augment more limited physical scaling?
- Research to develop new cost –effective fabrication technologies, perhaps based on self-assembly methods, to realize systems with component counts numbering in the billions.
- Research to eventually supersede current device scaling with molecular-scale devices that could offer enormous complexity and capability at greatly reduced levels of energy use.

IV. Outreach Activities

Immediately after the workshop, the workshop summary, agenda, and most of the presentations were placed on the SRC public website at http://www.src.org/research/iwfipt/3rd_iwfipt.dgw. Several Professors from universities in Asia, North America, and Europe were invited and attended the workshop. It is hoped that the discussions held at the workshop influenced their research programs and thereby indirectly influenced student researchers.

Planning is underway for the Fourth International Workshop on Future Information Processing Technologies that is to be held in Europe in September of 2001.

V. Journals, Books, Products, Other Contributions

The electronic materials contained at the above URL were the only planned publications from the workshop.